



Spin Transfer Technologies

An Allied Minds Company

\$22.8 million convertible bridge facility

Update on memory market and STT's powerful ST-MRAM technology

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Allied Minds introduction



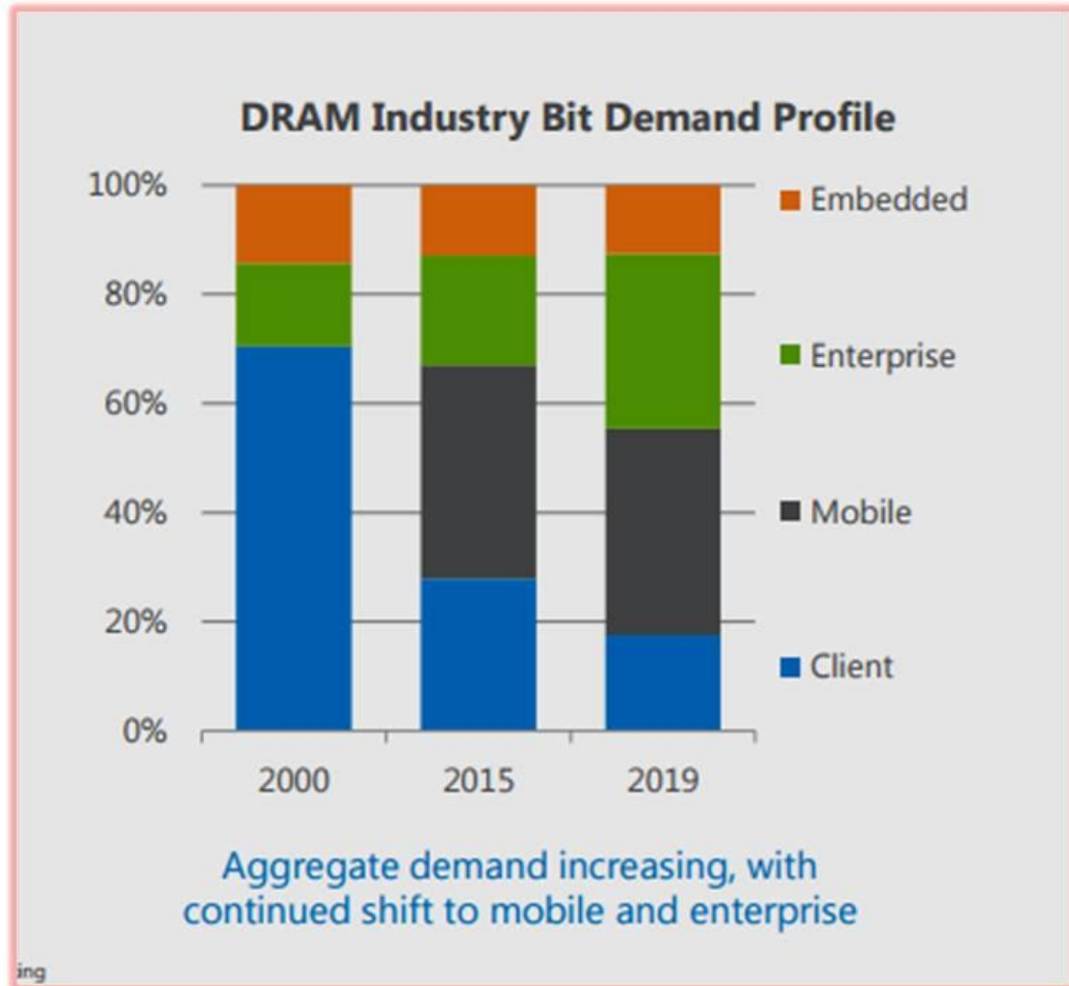
- \$22.8 million convertible bridge facility, underwritten by Allied Minds with other investors expected to participate
 - Bridge to Series B fund-raise planned for Q1 2018, expected to include new investors
- Extensive evaluation confirmed market opportunity, strength of STT's technical differentiation, team
 - External diligence by senior industry experts, potential customers, partners
 - STT's technologies have potential to enable MRAM to replace SRAM and DRAM (>\$20bn market opportunity)
 - Technologies, fab, patent protection and team position STT for success
- Under new CEO, STT on clear path to commercialization
 - Product roadmap, milestones to deliver commercial-grade MRAM
 - Potential customer, partner engagement underway
 - New additions to team, team aligned to deliver results
- Bridge provides run-way to deliver on early milestones and secure strategic partners for Series B fund-raise

Summary



- MRAM has potential to replace embedded SRAM and key DRAM segments
 - DRAM is \$20Bn market; limits of DRAM challenged, especially for enterprise and mobile
 - MRAM has potential to disrupt SRAM and DRAM markets
 - STT technology has potential to meet requirements for SRAM and DRAM replacement
- STT's differentiated technology and capabilities expected to enable meaningful performance advantages for its own and third party structures, in time for emerging market
 - Three core elements:
 - Smaller, faster pMTJ structures
 - Patented/Pending Spin Polarizer
 - Patented/Pending Endurance Engine
 - Fast turn, world-class Fabrication plant
 - Multi-disciplined, synergistic engineering team

Holy Grail: \$20B DRAM Market



- Enterprise and Mobile represent greatest opportunity – estimated \$20bn market
 - Fastest growing segments
 - Power, persistence and cost are most important
 - DRAM commands a price premium
 - DRAM reaching the physical limits of its capabilities; difficult to shrink further
- *MRAM has the potential to meet the needs of these markets*
 - *Lower power and lower cost*



DRAM is standard today, but has problems



- Advantages
 - Capacity: Gb's
 - Size: Efficient: small, cheap to make Gb's
 - Speed: Fast ~12ns
 - Endurance: Can be used 10^{15} times
- DRAM challenges:
 - Power consumption is high
 - Needs external circuits to work - extra power
 - Loses data on power loss/interruption
 - Structures struggling to get smaller
 - Battery back-up schemes expensive, clumsy



Memory in servers estimated to use as much power as City of San Francisco

MRAM has potential to disrupt memory market



- **Small** (key to memory dominance)
 - Can compete with DRAM sizes
 - MRAM ½ to ¼ size of SRAM
- **Lower Power** (far superior to DRAM – eg doubling smartphone life)
 - Uses no power when idle
 - Lower voltages
 - No external circuitry required
- **Non-Volatile** (key advantage over DRAM)
 - Needs no power to remember
 - Fastest “NV” in the world
- **Fast** (as fast as DRAM, even SRAM)
 - <10ns switching speeds demonstrated
 - Can replace DRAM, SRAM

	MRAM	SRAM	DRAM	Flash	FeRam
Read Speed	Fast	Fastest	Medium	Fast	Fast
Write Speed	Fast	Fastest	Medium	Slow	Medium
Array Efficiency	Med/High	High	High	Med/Low	Medium
Scalability	Good	Limited	Limited	Limited	Limited
Cell Density	Med/High	Low	High	Medium	Medium
Non-Volatility	Yes	No	No	Yes	Yes
Endurance	SPIN	Infinite	Infinite	Limited	Limited
Cell Leakage	Low	Med/High	High	Low	Low
Low Voltage	Yes	Yes	Limited	Limited	Limited
Complexity	Med/High	Low/Med	Medium	Med/High	Medium

So why hasn't MRAM disrupted already?

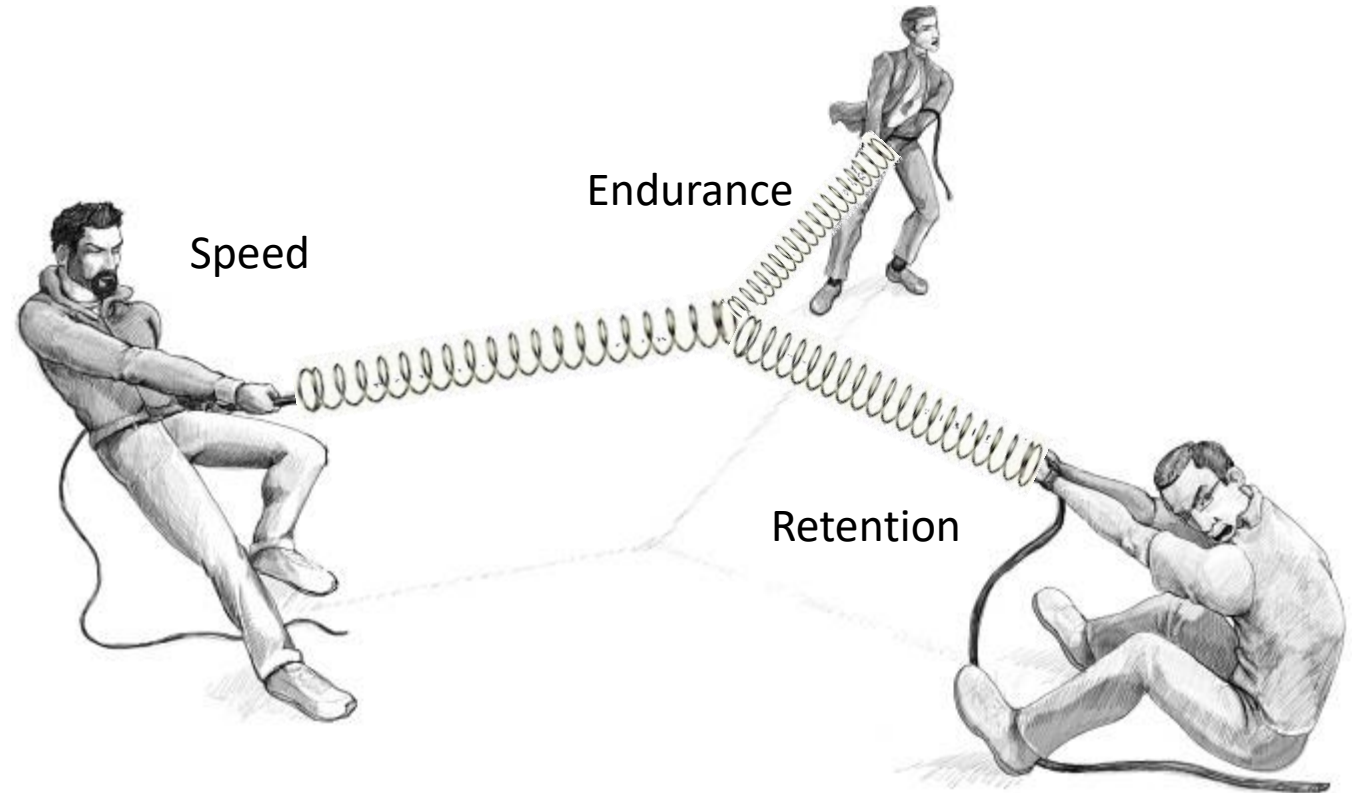


No one has solved the MRAM trade-off between endurance, speed and retention:

- Endurance $< 10^{10}$
- Speed $> 20\text{ns}$
- Retention good

Plus:

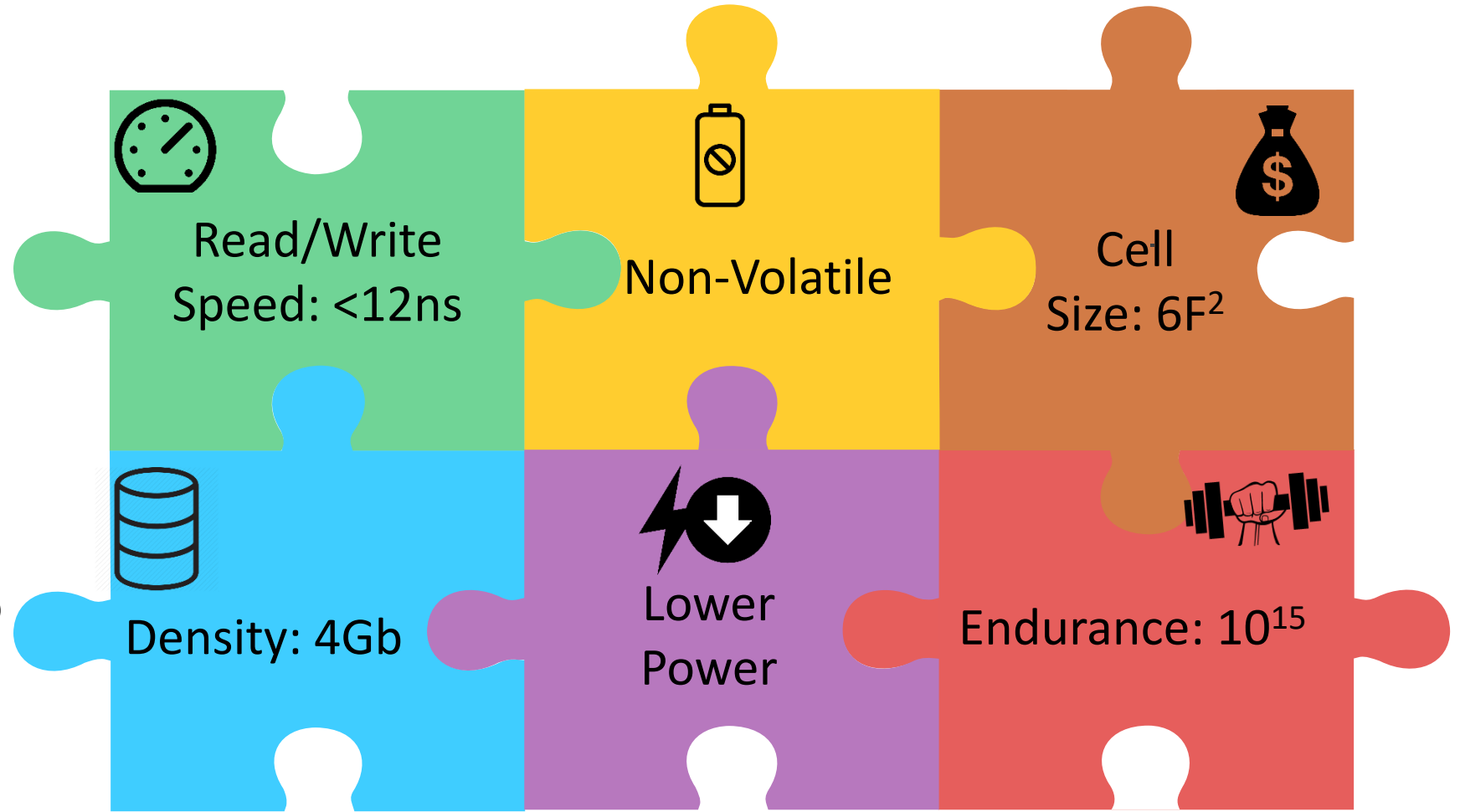
- Writing is “probabilistic”
- Sub 30nm tolerances difficult



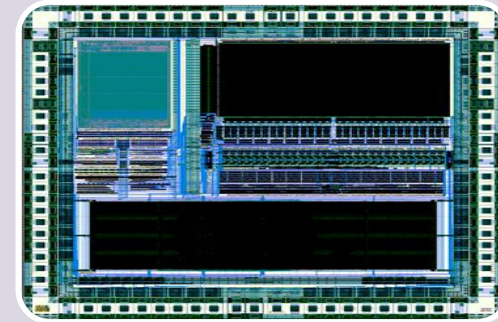
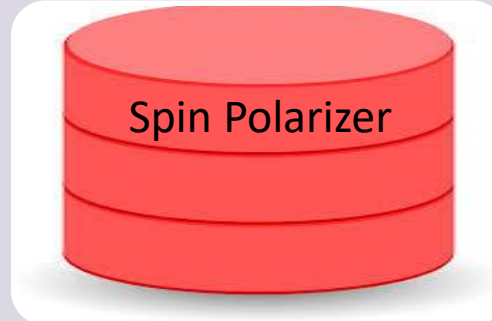
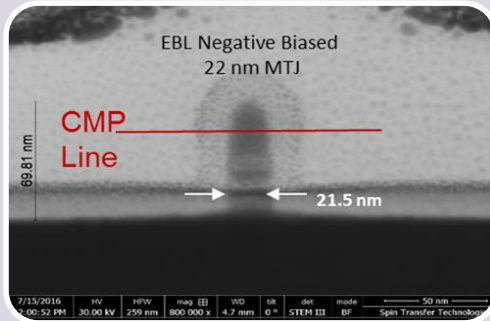
What's required to replace DRAM?



- MRAM is inherently non-volatile and low power
- STT's MRAM already meets DRAM speeds
- STT's technologies have the potential to unlock the other specifications



Design plan to unlock commercial grade MRAM



Smaller pMTJ

10ns speed
DRAM size
Gb densities
Compatible with
advanced semi-
processes

Patented pMTJ Enhancement

Faster Switching
Lowers R/W current
Critical for smaller
geometries
Heavily Patented

Endurance Engine

Increases endurance
by up to 6 orders of
magnitude
Eliminates R/W Errors
Shortens time to high
yield – potentially by
years

Why are we so excited?



- World-beating magnetics: proprietary pMTJ/Spin Polarizer combination
 - Provides material improvements to pMTJ efficiencies
 - pMTJ must be very small to compete with DRAM
 - As pMTJ shrinks, value of Spin Polarizer rises
 - Deterministic write onset
- “Endurance Engine” is proprietary design IP with unique degrees of freedom
 - Allows smaller write currents → smaller cells
 - Smaller cells → lower cost
 - Boost memory endurance by up to six orders of magnitude
 - Universal → potentially applicable to anyone’s pMTJ
 - Works on NVM, SRAM or DRAM
- Anticipate 100 patents by Q1 2018

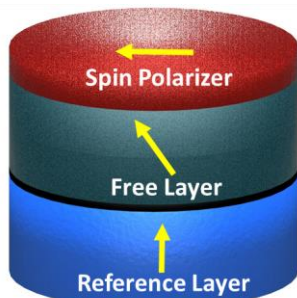
STT: combining magnetics + circuits

The path to persistent DRAM



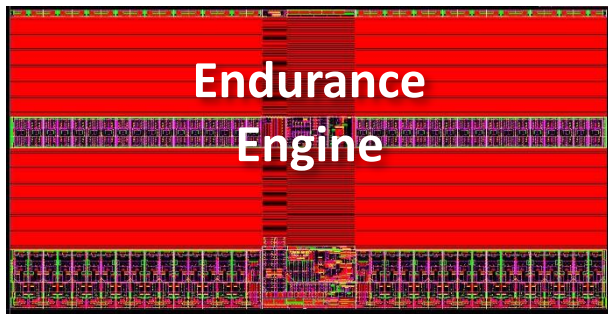
Capabilities

Benefits



Magnetics

+



Endurance
Engine

Easier to write
to memory

Lower power to
read memory

Faster to write
memory

Longer life of
memory
(endurance)

~ 10ns read/write cycle
DRAM/SRAM class

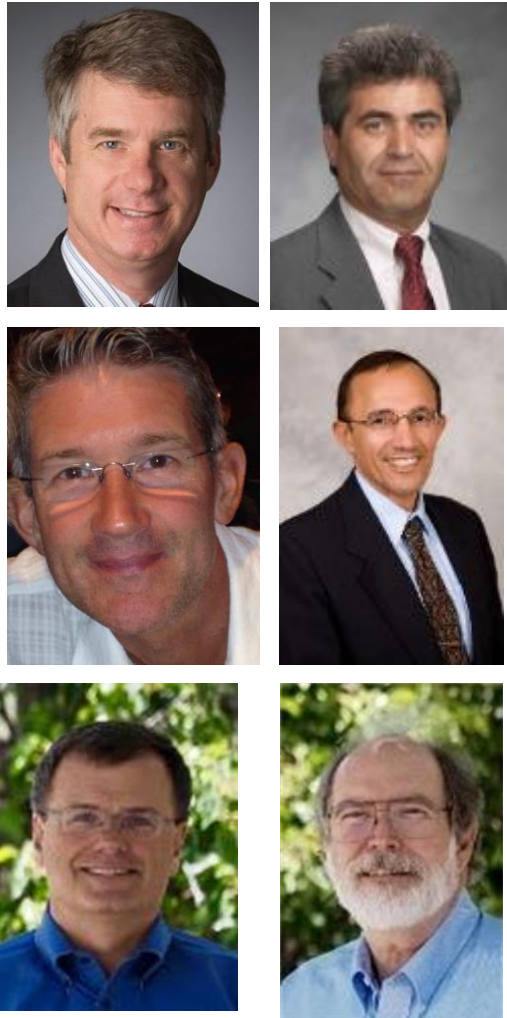
Lower write current → smaller
cell xistor → lower cost → DRAM

Lower write energy → DRAM

DRAM/SRAM-like
endurance > 10^{15}

Improved stability –
retention and RER for
persistent DRAM

World class executive team

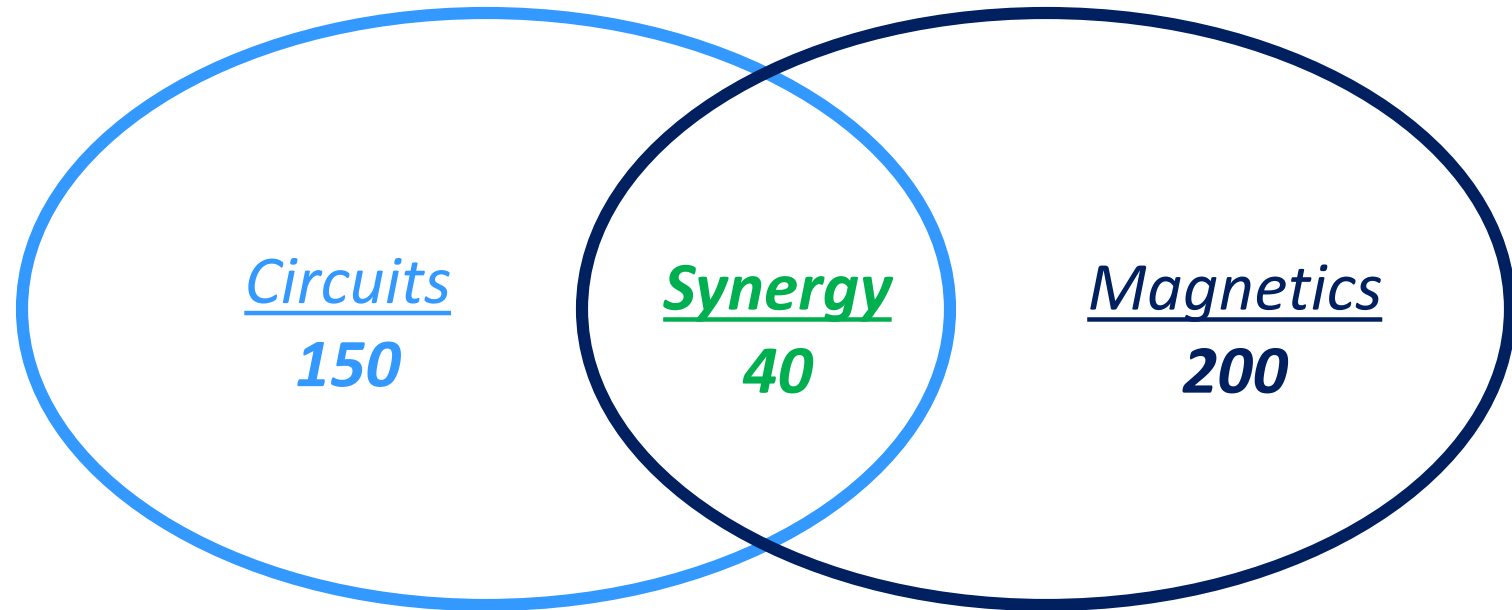


- **CEO: Tom Sparkman** – 35 years experience in medical, semiconductor and wireless technologies, including GM Analog BU (Japan) and SVP WW Sales at Spansion, Inc. Integrated Fujitsu Micro acquisition and key member of Exec team that sold Spansion to Cypress; SVP WW Sales and GM Comms BU at IDT, Founding CEO at Samplify, Early Employee and 19 years at Maxim. Founding member of Maxim Europe, six years in Munich
- **CTO, VP Magnetics Technology: Mustafa Pinarbasi, PhD** – 30+ years experience in thin film materials and magnetic thin film technologies, technology leadership positions at IBM, Hitachi Global Storage Technologies (HGST) and SoloPower, pioneered the development of GMR read sensor at IBM and TMR read head processing at HGST. Holds over 190 US patents
- **VP, Product: Andy Walker, PhD** – is a 30+ years experience in the semiconductor industry, including with Philips Research Laboratories, Eindhoven, Cypress Semiconductor, Artisan Components and Matrix Semiconductor. He has been involved with 3-D Flash memory technology since 2000 and founded Schiltron Corporation to investigate and develop new 3-D Flash technologies. Holds over 40 US patents
- **VP Memory Integration, Patent Strategy: Amitay Levi, PhD** – 30+ years experience in technology development of non-volatile memory, including Flash and MRAM. Developed technology from early start to high volume production in multiple foundries around the world
- **VP Business Development: Jeff Lewis** – 30+ years semiconductor experience, including Senior VP of Business Development and Marketing at SuVolta, Inc. and at Innovative Silicon, and additional roles as CEO of CiraNova, VP positions at FormFactor, Artisan Components and Compass Design Automation
- **VP IC Product Development: Les Crudele** – 40+ years semiconductor experience including VP & GM of Motorola's PowerPC RISC Division, VP & GM Compaq's Workstation Products, and CEO of Banderacom, Transmeta and Azuray. Holds 10 patents

400 man-years' engineering; own fab



- World class team with 15 PhD's. Total team of 40
- 200+ years magnetics experience; 120+ years of memory design experience
- Complete in-house engineering and physics teams
 - Physics
 - Electrical engineering
 - Thin-film engineering
 - Mechanical engineering
 - Test engineering
 - Reliability engineering
 - 3D memory design
- Complete manufacturing 8" MRAM Fab line



Next 6 months



- Q4 2017
 - 1G of characterization data on pMTJ collected
 - Competitive pMTJ
- Q1 2018
 - Filed / granted 100 patents
 - Emulator demo of Endurance Engine
 - FPGA demo of Endurance Engine
 - Confirmation of Spin Polarizer; 28nm pillar demo

Medium term STT goals



- Deliver commercial grade ST-MRAM in 2019 that meets SRAM specifications
- Substantial progress against DRAM specifications through 2018
- Deliver DRAM-grade ST-MRAM with partner in 2020 – targeting \$20 billion market segments
- Expect to generate revenue in 2018, with multiple revenue opportunities going forward through product and separate licensing of core technologies

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 - Patented/Pending Spin Polarizer
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 - Fast turn, world-class Fabrication plant
 - Multi-disciplined, synergistic engineering team
- \$22.8M bridge to Series B (Q1 2018) will fund achievement of material milestones and provide path to bringing in strategic investors

Glossary



- **MRAM** – Magnetic Random Access Memory. MRAM requires no power to retain data.
- **MTJ** – Magnetic Tunnel Junction
- **pMTJ** – Perpendicular Magnetic Tunnel Junction
- **SRAM** – Static Random Access Memory. SRAM requires power to retain data.
- **DRAM** – Dynamic Random Access Memory. DRAM requires power to retain data.
- **Non-Volatile Memory (NVM)** - Retains its data with power off
- **Volatile Memory** – Loses data with power off
- **1T1J** – Memory cell with 1 Transistor and 1 MTJ
- **Persistence** – Ability of a memory to retain data without power for a limited time
- **Endurance** – Number of write/erase cycles before memory becomes unusable
- **Retention** – Capability of memory to retain state without power after cycling and at higher temperature