Universal technologies enabling DRAM-grade MRAM
Unlocking the >$20bn+ DRAM market (Mobile & Enterprise)
Powering the next generation of applications
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STT: DRAM-grade MRAM
Universal, enabling technologies unlocking a $20bn+ market

<table>
<thead>
<tr>
<th>Market</th>
<th>DRAM: &gt;$20bn (Enterprise and Mobile alone)</th>
<th>Poised – subject to performance enhancements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>✔ Fast (~12ns)</td>
<td>✗ Limited (&gt;20ns)</td>
</tr>
<tr>
<td>Size</td>
<td>✔ Cell size 6F² (can’t be shrunk further)</td>
<td>✗ Limited [quantify]</td>
</tr>
<tr>
<td>Endurance</td>
<td>✔ High (10¹⁵)</td>
<td>✗ Limited (10⁸)</td>
</tr>
<tr>
<td>Power</td>
<td>✗ High consumption</td>
<td>✔ Low consumption</td>
</tr>
<tr>
<td>Volatile?</td>
<td>✗ Volatile</td>
<td>✔ Non-volatile (persistent)</td>
</tr>
</tbody>
</table>

Solution: enabling, universal technologies potentially applying to all MRAM variants:
1. Spin Polarizer
2. Endurance Engine
3. 3D / MLC
STT’s 3 patented, universal technologies
Potential to solve MRAM’s endurance, size and speed limitations

Endurance Engine  pPMTJ + Spin Polarizer  3-D/MLC
(circuitry)  (magnetics)  (synergy)

• Up to $10^6$ endurance boost
• Potentially compatible with any MTJ
• Increases yields
• 30-40 patents*
• Parallels to SanDisk

• Up to 30% efficiency increase
• Shrinks array size
• Speeds switching
• 30-40 patents*
• From NYU Initially

• “MLC” MRAM
• 3-D MRAM
• Smaller geometries
• Testing/reliability
• Synergy
• 30-40 Patents*

* Patents + Patent Pending
## Enhancing MRAM performance

Addressing IoT, mobile and Enterprise segments

<table>
<thead>
<tr>
<th></th>
<th>IoT</th>
<th>Mobile Computing</th>
<th>Data Centers/LPDRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Endurance</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Speed</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Size</td>
<td>✕</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Non volatile</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Execute-in-Place</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Current MRAM</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Spin’s Technology</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>eSRAM (cache)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Current MRAM</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Spin’s Technology</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>DRAM &amp; LP-DRAM</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Current MRAM</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Spin’s Technology</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

### TAM:
- Emerging: $500M
- $500M
- $20B+
MRAM performance enhancement journey
30 – 50% – key to competitiveness for all providers

STT targeting enhancements that unlock critical performance gains

<table>
<thead>
<tr>
<th>Commercial availability (year)</th>
<th>Current</th>
<th>2018</th>
<th>2019</th>
<th>2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAM</td>
<td>$250M</td>
<td>$500M</td>
<td>$1Bn</td>
<td>$20Bn</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Speed</th>
<th>45ns</th>
<th>15ns</th>
<th>10ns</th>
<th>10ns</th>
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<tbody>
<tr>
<td>Endurance</td>
<td>10^8</td>
<td>10^13</td>
<td>10^14</td>
<td>10^14</td>
</tr>
<tr>
<td>Cell Size</td>
<td>40F^2</td>
<td>30F^2</td>
<td>30F^2</td>
<td>5F^2</td>
</tr>
<tr>
<td>Power</td>
<td>100%</td>
<td>80%</td>
<td>60%</td>
<td>60%</td>
</tr>
<tr>
<td>Density</td>
<td>1-10MB</td>
<td>16M-1G</td>
<td>256M-1G</td>
<td>4G-8G</td>
</tr>
<tr>
<td>Retention</td>
<td>10 yrs</td>
<td>1 week</td>
<td>1 day</td>
<td>1 day</td>
</tr>
<tr>
<td>Change Magnetics</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Process</td>
<td>Standard</td>
<td>Standard</td>
<td>Standard</td>
<td>DRAM</td>
</tr>
</tbody>
</table>

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Market opportunity exceeds $20bn
Starting with SRAM in 2019; DRAM 2021

Step One: SRAM-Replacement - 2019
- Prove technology quickly by leveraging existing solutions at foundries
- Stand-alone/embedded SRAM Replacement
- Licensed to foundries/IDMs/partners
- $500m TAM
- Critical component of ~$80B semi market

Step Two: Persistent DRAM - 2021
- Holy Grail of memory opportunities
- Revolution in computer architectures
- Key to IoT, AI, HPC, Mobile, etc. advances
- Product ~$20B+ TAM
MRAM: the EMERGED next-gen memory
Market for STT’s MRAM enabling solutions already exists

3 foundries shipping MRAM next year as NVM (flash) replacement
– TSMC – Multiple nodes; advanced nodes
– Samsung – NXP/Qualcomm Partner
– GlobalFoundries – Everspin Partner

All other foundries beginning MRAM
– Potential market for all of STT’s offerings

Extensive work at other companies, e.g.
– SK Hynix + Toshiba – DRAM replacement
– Intel – NVM Memory
– Qualcomm – Cache memories

MRAM EcoSystem Exists
– Magnetics is a solvable problem
– Advanced Tools Exist. TEL Leads the pack.
– Materials, Know-How
### Core Technology

**Complete FPGA demo for the Endurance Engine on real MRAM memory arrays**

Demonstrate 30%+ benefits of Spin Polarizer

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### Engine Block; Depot Tool

Tape out first blocks of Endurance Engine in 22nm CMOS process in cooperation with Foundry Partner.

Install MRAM deposition tool at Spin Fab line in Fremont

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### Real Silicon

Evaluate first silicon on Endurance Engine

Demonstrate 28nm MTJ, Spin Polarizer at 400°C

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### World’s Best MTJ

Final Tape out Endurance Engine as working 64M SRAM product.

Smallest, high-speed MTJ + Spin Polarizer

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### Risk Retired

Sample working 64M Persistent SRAM product to market. Begin qualification for production.

Install MTJ/ Spin Polarizer at Foundry Partner

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**Q1 18**
- Proving performance claims in the lab
- Potential for substantial technology risk retirement by H1 2019

**Q2 18**
- Complete FPGA demo

**Q3 18**
- Tape out first blocks

**Q4 18**
- Final Tape out

**Q1 19**
- Sample working 64M Persistent SRAM product
Ecosystem strategy
Partnering to commercialise DRAM grade MRAM by 2021

• System Beneficiaries
  – Technology leaders would be key partners, technology drivers
  – Non-volatile memory holds potential to revolutionize their architectures, with radical advances in compute power and reductions in power consumption
  – Apple, Google, Amazon, Arm, Qualcomm, Huawei, Tencent, Alibaba, Fujitsu, etc

• Memory and Semi Companies
  – Medium-sized memory (Cypress, ISSI, Giga, etc.) – MRAM potential key to strategies
  – Larger DRAM companies (Samsung, Hynix, Micron, etc.) want cost, density. STT potentially has all the pieces
  – MCU Companies want <28nm embedded memory solution. Intel, ST, Microchip, Renesas, Avago, etc
  – SoC Companies want <28nm SRAM solution. Apple, Samsung, Qualcomm, Avago, etc

• Foundries (TSMC, SMIC, UMC)
  – No solution for Flash and SRAM below 28nm. This is a major issue for the entire industry
  – All must have MRAM technology
  – MRAM must be “easy.” Engine does that. We can potentially sell to all of them, even competitors

• China, Inc.
  – Tremendous amount of wafer capacity being built now. What will they use it for?
  – China, Inc. has limited access to DRAM. No access to 3D NAND. MRAM the only path?
  – Memory arguably is the only thing big enough to fill these huge fabs
How has “little old” STT achieved this?

Time/IP
- STT founded in 2006 on spin polarizer technology sourced from NYU – we’ve been at it a long time!

Capital
- $121m invested to date
- Delivering a proprietary Fab – far superior cycle times

Experts
- World class magnetics and circuitry teams – 22 PhDs
- Synergistic collaboration between the two
  - Purist focus on scientific R&D in early years (now commercially targeted)

Focus
- Holistic, system based approach, focusing on the end-user view

Partnerships
- TEL: leading producer of MRAM manufacturing tools globally
- STT/TEL collaborative engineering agreement gives STT early access to TEL equipment and engineering resource, further accelerating cycle times beyond peers’
Unlocking a premium exit valuation

| Disruptive innovation solving an important problem | • Inherently non-volatile + lower power consumption  
| • Particularly suited to fastest growing Mobile and Enterprise segments – low power consumption critical  
| • Advances in DRAM are capped out by physics |
| Favourable market dynamics | • Mobile and Enterprise DRAM segments: >$20bn; growing fast  
| • 2018 the “year of MRAM”  
| • Semiconductor stocks at record highs. Lots of cash |
| Sustainable competitive advantage | • >100 patents in place covering 3 key technologies  
| • R&D Fab and TEL agreement: superior cycle times |
| Route to widespread adoption | • Scope for licensing model  
| • Separate technologies can be licensed by field of use |
| Capable management, with aligned interests | • Semiconductor veterans  
| • Right blend of commercial and scientific experience |
| Establish potential for competitive tension | • DRAM incumbents need an MRAM solution  
| • We believe that only STT’s technology can unlock DRAM-grade MRAM |
Come see for yourself!
45500 Northport Loop West, Fremont CA 94538
Reference materials
World Class Executive Team

• **CEO: Tom Sparkman** – 35 years experience in medical, semiconductor and wireless technologies, including GM Analog BU (Japan) and SVP WW Sales at Spansion, Inc. Integrated Fujitsu Micro acquisition and key member of Exec team that sold Spansion to Cypress; SVP WW Sales and GM Comms BU at IDT, Founding CEO at Samplify, Early Employee and 19 years at Maxim. Founding member of Maxim Europe, six years in Munich.

• **CTO, VP Magnetics Technology: Mustafa Pinarbasi, PhD** – 30+ years experience in thin film materials and magnetic thin film technologies, technology leadership positions at IBM, Hitachi Global Storage Technologies (HGST) and SoloPower, pioneered the development of GMR read sensor at IBM and TMR read head processing at HGST. Holds over 190 US patents.

• **VP, Product: Andy Walker, PhD** – is a 30-year-plus veteran of the semiconductor industry. He was with Philips Research Laboratories, Eindhoven, Cypress Semiconductor, Artisan Components and Matrix Semiconductor. He has been involved with 3-D Flash memory technology since 2000 and founded Schiltron Corporation to investigate and develop new 3-D Flash technologies. He has over 40 US patents to his name.

• **VP Memory Integration, Patent Strategy: Amitay Levi, PhD** – more than 30 years experience in technology development of non-volatile memory, including Flash and MRAM. Developed technology from early start to high volume production in multiple foundries around the world.

• **VP Business Development: Jeff Lewis** – 30+ years semiconductor experience, including Senior VP of Business Development and Marketing at SuVolta, Inc., the same role at Innovative Silicon, and additional roles as CEO of CiraNova, and VP positions at FormFactor, Artisan Components and Compass Design Automation.

• **VP IC Product Development: Les Crudele** – 40+ years semiconductor experience including executive and technical leadership roles, including VP & GM of Motorola’s PowerPC RISC Division, VP & GM of Compaq’s Workstation Products, and CEO of Banderacom, Transmeta and Azuray. Holds 10 patents.
What is ST-MRAM?

- MRAM is **Magneto-resistive RAM**
  - Magnetic polarization sets ‘1’, ‘0’
- STT is **Spin Transfer Torque**
  - Electron spin sets Free Layer polarization
  - ST-MRAM using pMTJ is latest MRAM generation
- Bitcell uses 1 transistor + 1 MTJ
  - Very dense configuration
- Attributes:
  - Non-volatile
  - High-speed read and write
  - High endurance
  - Easy integration in BEOL – no impact on FEOL

![Perpendicular Magnetic Tunnel Junction (pMTJ)](image)
Glossary

• **MRAM** – Magnetic Random Access Memory. MRAM requires no power to retain data.
• **MTJ** – Magnetic Tunnel Junction
• **pMTJ** – Perpendicular Magnetic Tunnel Junction
• **SRAM** – Static Random Access Memory. SRAM requires power to retain data.
• **DRAM** – Dynamic Random Access Memory. DRAM requires power to retain data.
• **Non-Volatile Memory (NVM)** - Retains its data with power off
• **Volatile Memory** – Loses data with power off
• **1T1J** – Memory cell with 1 Transistor and 1 MTJ
• **Persistence** – Ability of a memory to retain data without power for a limited time
• **Endurance** – Number of write/erase cycles before memory becomes unusable
• **Retention** – Capability of memory to retain state without power after cycling and at higher temperature